AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1. (Original) A method for configuring a routing program for routing connections between an integrated circuit device and an embedded core, comprising:

obtaining a first horizontal pitch and a first vertical pitch for one of the integrated circuit device and the embedded core;

obtaining a second horizontal pitch and a second vertical pitch for the other of the integrated circuit device and the embedded core, the first vertical pitch and the second vertical pitch being different;

inputting a first connection layer input to the routing program, the first connection layer input including the first vertical pitch and a horizontal direction; and

inputting a second connection layer input to the routing program, the second connection layer input including the second horizontal pitch and a vertical direction.

Claim 2. (Original) The method of Claim 1 wherein the one of the integrated circuit device and the embedded core is a programmable logic device.

Claim 3. (Original) The method of Claim 2 wherein the other of the integrated circuit device and the embedded core is a microprocessor core.

Claim 4. (Original) The method of Claim 3 wherein the programmable logic device is a field programmable gate array.

Claim 5. (Original) The method of Claim 4 wherein the field programmable gate array and the microprocessor core are formed as separate integrated circuits which are interconnected, the field programmable gate array having a first plurality of metal layers, the microprocessor core having a second plurality of metal layers, at least one layer of the first plurality of metal layers having the first horizontal pitch and the first vertical pitch, and at least one layer of the second plurality of metal layers having the second horizontal pitch and the second vertical pitch.

Claim 6. (Original) A method for configuring a routing program for routing to an integrated circuit device having an embedded core, comprising:

providing a first horizontal pitch and a first vertical pitch for one of the integrated circuit device and the embedded core;

providing a second horizontal pitch and a second vertical pitch for the other of the integrated circuit device and the embedded core, the first horizontal pitch and the second horizontal pitch being different;

inputting a first connection layer input to the routing program, the first connection layer input including the first horizontal pitch and a vertical direction; and

inputting a second connection layer input to the routing program, the second connection layer input including the second vertical pitch and a horizontal direction.

Claim 7. (Original) The method of Claim 6 wherein the one of the integrated circuit device and the embedded core is a programmable logic device.

Claim 8. (Original) The method of Claim 7 wherein the other of the integrated circuit device and the embedded core is a microprocessor core.

Claim 9. (Original) The method of Claim 8 wherein the programmable logic device is a field programmable gate array.

Claim 10. (Original) The method of Claim 9 wherein the field programmable gate array and the microprocessor core are formed as separate integrated circuits which are interconnected, the field programmable gate array having a first plurality of metal layers, the microprocessor core having a second plurality of metal layers, at least one layer of the first plurality of metal layers having the first horizontal pitch and the first vertical pitch, and at least one layer of the second plurality of metal layers having the second horizontal pitch and the second vertical pitch.

Claim 11. (Original) An integrated circuit device, comprising:

a first device coupled to a second device;

the first device comprising a first horizontal pitch and a first vertical pitch;

the second device comprising a second horizontal pitch and a second vertical pitch; and

at least one interconnect layer for coupling the first device and the second device, the interconnect layer comprising a set of pitches selected from:

(i) the first vertical pitch and the second horizontal pitch; and

(ii) the first horizontal pitch and the second vertical pitch.

Claim 12. (Original) The integrated circuit device of Claim 11 further comprising a plurality of logic blocks for interconnecting the first device and the second device.

Claim 13. (Original) The integrated circuit of Claim 12 wherein the first device is a programmable logic device.

Claim 14. (Original) The integrated circuit of Claim 13 wherein the programmable logic device is a field programmable gate array.

Claim 15. (Original) The integrated circuit of Claim 13 wherein the second device is a microprocessor core.

Claim 16. (Original) The integrated circuit of Claim 15 wherein the microprocessor core is embedded in the programmable logic device.

Claim 17. (Original) The integrated circuit of Claim 16 wherein the programmable logic device comprises more metal interconnect layers than the microprocessor core.

Claim 18. (Original) The integrated circuit of Claim 11 wherein the second device comprises a plurality of pins for interconnection thereto.

Claim 19. (Original) The integrated circuit of Claim 11 wherein the interconnect layer was routed using a routing program having as inputs the set of pitches.

Claim 20. (Original) The integrated circuit of Claim 19 wherein the set of pitches is divided for input to the routing program, wherein one pitch in the set of pitches is for one metal layer and the other pitch in the set of pitches is for another metal layer.

Claim 21. (Original) A system, comprising:

an external memory circuit having one or more configuration data output terminals; and

a programmable logic device (PLD), the PLD comprising:

a programmable logic portion having a first vertical pitch and a first horizontal pitch;

an internal configuration memory having one or more configuration data input terminals coupled to the configuration data output terminals of the external memory circuit, and further having output terminals coupled to the programmable logic portion of the PLD;

an embedded core having a second vertical pitch and a second horizontal pitch, wherein the first vertical pitch and the second vertical pitch are different; and

a first interconnect layer coupled between the programmable logic portion of the PLD and the embedded core, the first interconnect layer having a set of pitches selected from:

(i) the first vertical pitch and the second horizontal pitch; and

(ii) the first horizontal pitch and the second vertical pitch.

Claim 22. (Original) The system of Claim 21, wherein the external memory circuit comprises one of a group of integrated circuits comprising: an EEPROM, an EPROM, and a PROM.

Claim 23. (Original) The system of Claim 21, wherein the programmable logic portion of the PLD is a field programmable gate array (FPGA).

Claim 24. (Original) The system of Claim 21, wherein the embedded core is a microprocessor.

Claim 25. (Original) The system of Claim 21, wherein the interconnect layer was routed using a routing program having as an input the set of pitches.

Claim 26. (Original) The system of Claim 25, wherein the PLD comprises a second interconnect layer coupled between the programmable logic portion of the PLD and the embedded core.

Claim 27. (Original) The system of Claim 26, wherein the set of pitches is divided for input to the routing program, wherein one pitch in the set of pitches is used for the first interconnect layer and the other pitch in the set of pitches is used for the second interconnect layer.

Claim 28. (Original) The system of Claim 21, wherein the first horizontal pitch and the second horizontal pitch are also different.